SPI 2024

28th IEEE Workshop on Signal and Power Integrity

May 12-15, 2024
Lisbon, Portugal

Proceedings

IEEE
IEEE ELECTRONICS PACKAGING SOCIETY
EMC SOCIETY
MTT-S IEEE MICROWAVE THEORY & TECHNOLOGY SOCIETY
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Dear colleagues and friends,

We are glad to present the Proceedings of the **28th IEEE Workshop on Signal and Power Integrity**!

Held during May 12-15, 2024, this year's SPI edition took place in Lisbon, so for the second time a Portuguese city had the honor of hosting this noteworthy event that stands for almost three decades as a forum of exchange on all aspects of Signal and Power Integrity, comprising the latest research and developments on design, characterization, modeling, simulation and testing at chip, package, board, and system level.

Bringing together 87 participants from 19 countries spread throughout 3 continents, the **SPI 2024** technical program upheld the international high-quality projection that has been the hallmark of this series of conferences: 24 oral and 11 poster presentations divided between 7 oral and 1 poster sessions, alongside 1 tutorial and 3 keynotes delivered by our invited speakers Lorenzo Codecasa, Rajen Murugan, Cian Ó Mathúna and Kemal Aygün, all standing as renowned names in the fields of Academia and Industry, and finally an Industry Forum organized by the Industry Advisory Board that joined panelists from 5 eminent worldwide companies.

The **SPI 2024 Awards and Grants** were also an important feature during the workshop, aiming to encourage all participants and especially graduate students to attend and present their current research developments. Congratulations to Riccardo Trinchero, Tommaso Bradde, Mihai Telescu and Igor Simone Stievano for winning the *Best Paper Award*, to Tim Pattyn for winning the *Best Student Paper Award* and an IEEE EPS *Student Travel Grant*, and to Morten Schierholz for winning an IEEE EPS *Student Travel Grant*.

Beyond the scientific matters, and in accordance with the long-standing tradition of this workshop, the social events were carefully prepared to offer everyone a pleasant sightseeing of Portugal's historical capital city, as well as a glance of the country's rich gastronomy: from the City Tour that visited some magnificent 16th century national monuments nowadays classified as UNESCO World Heritage Sites, to a Gala Dinner set in a charming ballroom inside a modernized palace first built in the late 17th century, our participants enjoyed quite a few remarkable surprises!

Foreword

On behalf of the entire **SPI 2024** Organization, we express our gratitude to the Institute of Telecommunications as hosting Institution; thank you also to our invited speakers for their kind availability and to all authors whose work is the basis for this workshop; a sincere word of appreciation is due to the sponsoring IEEE societies – EPS, EMCS and MTT-S – and to our private sponsors, who helped make possible this event with their active support; last but not least, an acknowledgement to the technical staff and the workshop volunteers for their valuable assistance.

To all **SPI 2024** participants, we hope the workshop fulfilled your expectations and you had a wonderful time while in Lisbon! Join us again for the next SPI workshop, to be held from May 11-14, 2025, in Gaeta, Italy!

Joana Catarina Mendes, SPI 2024 Workshop Chair

Antonio Maffucci & *Stefano Grivet-Talocia*, SPI 2024 Program Chairs

Best Paper Award

Riccardo Trinchero[(1)], **Tommaso Bradde**[(1)], **Mihai Telescu**[(2)], **Igor Simone Stievano**[(1)]

[(1)]Politecnico di Torino, Italy; [(2)]Univ. Brest, CNRS, France

Modeling of IC Buffers from Channel Responses via Machine Learning Kernel Regression

Best Student Paper Award

Tim Pattyn

Ghent University, Belgium

Differential Interconnects with Integrated Equalization and Common-Mode Filtering for Broadband Signal Integrity Enhancement in High-Speed PAM-4 Signaling

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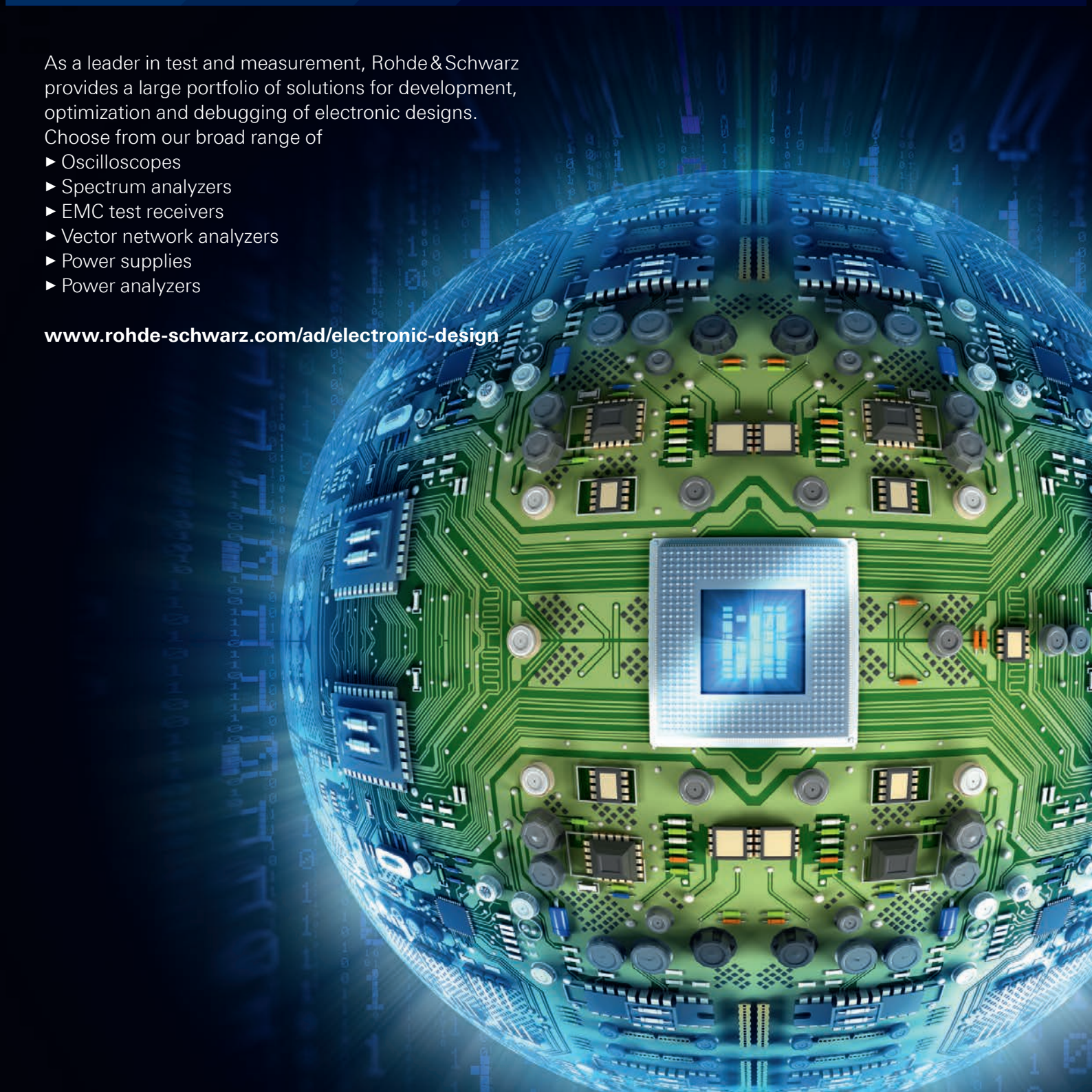


14:00 – 14:50 **Registration @ Venue**

GPS: 38.76495 -9.09779

14:50 – 15:00 **Tutorials Welcome**

15:00 – 16:00
16:30 – 17:30

TUTORIAL

16:00 – 16:30
Coffee-Break

Thermal Modeling of Electronic Components and Packages

Nowadays we are witnessing an ever-increasing need of thermal characterisation of electronic components and packages.

Firstly, in this tutorial it will be shown how electrical networks modeling electronic circuits can be coupled to properly defined thermal networks in order to derive electro-thermal networks able to accurately model thermal effects in electronic circuits by SPICE-like simulation.

Precisely, a physical-based definition of junction temperatures of electronic components will be introduced. It will be shown that this definition of junction temperature leads to thermal networks that preserve the thermodynamic properties of heat conduction equations in electronic devices and can be represented by passive RC multi-ports. A Model Order Reduction (MOR) approach tailored for these thermal networks, implemented in the code FAst Novel Thermal Analysis Simulation Tool for Integrated Circuits (FANTASTIC) and now available in commercial software, will be shown to allow a very efficient extraction of Compact Thermal Models (CTMs), and to approximate with any a priori error bound the port responses of the thermal networks. The application of this tool to state-of-the-art electronic case studies will also be presented in detail.

Secondly, in this tutorial it will be shown how such results on CTMs have been extended for the extraction of Boundary Condition Independent (BCI) CTMs for Computational Fluid Dynamics electronic cooling simulation.

Precisely, the notion of junction temperature will be shown to allow also the modeling of the boundary of electronic components or packages, in such a way to allow to model the coupling of the electronic component or package to all surrounding environments. This approach allows to overcome previous approach based on DELPHI-liked CTMs. Its implementation in the FANTASTIC BCI code, now also available in commercial software, will be shown by applications to state-of-the-art electronic case studies.

Several derivations of previous results will also be presented. In particular, it will be shown how to exploit in practical applications the structure function defining the RC transmission line model equivalent to a one-port thermal network, coming from the definition of junction temperature. Also, it will be shown how the presented approach to extract CTMs has been extended to extract parametric models, very useful for calibration, and to extract nonlinear models, crucial for power electronic circuits.

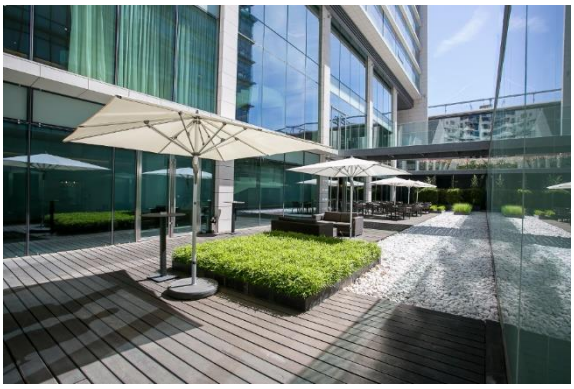
Lorenzo Codecasa

Politecnico di Milano, Milan, Italy

Lorenzo Codecasa received the Ph.D. degree in electronics engineering from Politecnico di Milano, Milan, Italy, in 2001. Since 2002, he has been working as an Assistant, then as an Associate, and lastly as a Full Professor of electrical engineering with the DEIB Department of the same University. In his research areas, he has authored or coauthored more than 250 articles in refereed international journals and conference proceedings. His main research contributions are in the theoretical analysis and the computational investigation of electronic circuits and electromagnetic fields. In Stanford University's ranking, he is listed as one of the world's 2% most influential scientists. He is particularly active in the research of heat transfer and thermal management of electronic components and packages, in which he has been introducing original approaches to the extraction of compact thermal models. Some of these techniques are becoming available in market-leading commercial software. Dr. Codecasa received the Harvey Rosten Award for Excellence (twice) in 2015 and 2022 and three best papers awards at THERMINIC in 2014, 2017, and 2019. He is currently an Associate Editor for IEEE TRANSACTIONS ON COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY. He has served as a Program Chair, the Vice-General Chair, and the General Chair of THERMINIC.

18:00 onwards **Welcome Reception**

***Olissippo Oriente* Hotel**



09:00 – 09:30 **Registration @ Venue**

09:30 – 09:50 **Opening Session**

09:50 – 10:30 **KEYNOTE**

Multiphysics and Multidomain Modeling of Semiconductor IC Packaging and Systems

Transistor/chip scaling has reached the point of diminishing returns and is becoming more complex and expensive at each node. Advanced packaging technologies show promise by bridging the gap in the "More than Moore" Era. However, advanced packaging technologies challenge traditional package design verification tools and methodologies. Complex miniaturization and integration exacerbate coupled multiphysics (e.g., electrical, thermal, mechanical) and multidomain (chip-package-PCB system) interactions. As such, without a paradigm shift in the traditional design verification modeling approach, potential business impacts are highly likely (viz costly re-spins, increased design cycle time, and time-to-market). Coupled multiphysics and system co-design (MSC-D) is emerging as the renewed modeling methodology to ensure first-pass design success.

This presentation reviews the development and implementation of an MSC-D methodology for designing high-performance, cost-effective IC complex packaging solutions. The methodology is validated against silicon laboratory measurements on two IC current sensor types – a precision shunt resistor sensor and a high-precision, high-voltage (600V) Hall-Effect current sensor. State-of-the-art progress, challenges, and opportunities in multiphysics system co-design are also discussed.

Rajen Murugan

Texas Instruments, Inc., Dallas (TX), USA

Dr. Rajen Murugan specializes in developing multiphysics system co-design simulation and modeling methodologies for advanced IC packaging and systems. He is currently a Distinguished Member of the Technical Staff (DMTS) with Texas Instruments, Inc. He has 31 granted (US and Canada) patents and 62 under review at the USPTO. He has published over 50 papers in peer-reviewed IEEE journals and conferences. Dr. Murugan holds a Ph.D. in Applied Electromagnetics from the University of Manitoba, Canada. He is an Affiliate Assistant Professor with the University of Washington EE Department, a Distinguished Lecturer for the IEEE Electronics Packaging Society (EPS), an Associate Editor for the IEEE Transactions on CPMT journal, a Senior Member of IEEE, the founder of the IEEE EPS Dallas Chapter, and the Chair of the IEEE Dallas Section (Region 5).

10:30 – 11:00 **Coffee-Break**

SESSION 1

11:00 – 12:20 **POWER DISTRIBUTION NETWORKS**

Chair: Heidi Barnes

11:00

Judy Amanor-Boadu, E Hammond

Intel Corporation, USA

Leveraging SIMPLIS to Better Predict Server Platform Power Delivery Performance

11:20

Morten Schierholz (1), Zouhair Nezhi (2), Marcus Stiemer (2), Christian Schuster (1)

(1) Hamburg University of Technology, Germany; (2) Helmut Schmidt University, Germany

PCB based Power Deliver Network Analysis Using Transfer Learning and Artificial Neural Networks

11:40

Youcef Hassab, Morten Schierholz, Christian Schuster

Hamburg University of Technology, Germany

Application of Gaussian Process Regression for Data Efficient Prediction of PCB-based Power Delivery Network Impedance Features

12:00

Antonio Carlucci, Tommaso Bradde, Stefano Grivet-Talocia

Politecnico di Torino, Italy

Fast Prediction of Worst-Case Voltage Droops in Power Distribution Networks

12:20 – 12:30 **SPONSOR PITCH**

Victor Medina – *Rohde & Schwarz, Portugal & Spain*

12:30 – 14:00 **Lunch**

14:00 – 14:40 **KEYNOTE**

MagIC – Making Magnetics Disappear onto Silicon Enabling Power Supply on Chip (PwrSoC) and Power Supply in Package (PwrSiP)

The trend in power delivery for processors and other complex SOC platforms is moving away from Point of Load (POL) power to integrated voltage regulation (IVR). This is facilitating the concept of granular power whereby large arrays of dc-dc converters are integrated within the processor package thereby enabling dramatic reduction in overall system energy.

This paradigm shift has been enabled by the dramatic miniaturisation of magnetic inductors using thin-film magnetic cores on silicon and PCB-embedded structures to replace bulky wire-wound devices.

This talk will discuss the commercial emergence of magnetics-on-silicon technology (MagIC) and associated PCB-embedded magnetics technologies which are enabling Power Supply on Chip and Power Supply in Package platforms.

This emerging space of vertical power delivery is transforming the industry ecosystem for processor and SOC power management. It is also being enabled by the recent focus on Heterogeneous Integration and Chiplet platforms for 2.5D and 3D packaging as evidenced in the EU Chips Act and the USA Chips Act.

The technologies will be introduced along with the performance capabilities and improvements over conventional magnetics and Point of Load power. The discussion will also consider Heterogeneous Integration of these components with processors using 2.5D and packaging and the emerging Micro Transfer Printing.

Cian Ó Mathúna

Tyndall National Institute, University College Cork, Ireland

Cian Ó Mathúna is Head of MicroNano Systems at Ireland's Tyndall National Institute. His research, over three decades, into the miniaturisation and integration of magnetics onto silicon, has played a key role in disruptive developments in integrated power management for processors in portable electronics and high performance computing. Using semiconductor processing of thin-film magnetics, Ó Mathúna's team have made bulky power magnetic components disappear onto silicon chips. Referred to as MagIC, Tyndall's magnetics-on-silicon technology has been licensed to two of the world's leading consumer electronics companies as well as a leading semiconductor foundry. In 2008, Ó Mathúna founded the International Workshop on Power Supply on Chip (PwrSoC) which has become a highly-influential flagship workshop for IEEE Power Electronics Society and US-based Power Sources Manufacturers Association (PSMA). Through his leadership, and his extensive collaborations with world-leading industry players in Europe, USA and Asia, Ó Mathúna has had a significant influence on the emergence of a global supply-chain for PwrSoC that, in 2021, has seen high-volume production of magnetics-on-silicon in commercial product. Prof. Ó Mathúna is an IEEE Fellow and, in 2021, received the IEEE Power Electronics Society Technical Achievement Award for Integration and Miniaturisation of Switching Power Converters and also received an EARTO (European Association of Research and Technology Organisations) Impact Innovation Award.

SESSION 2

14:40 – 15:40 **MODELS AND METHODS FOR SI/PI ANALYSIS**

Chair: Jose Schutt-Aine

14:40

Tim Pattyn, Arno Moerman, Martijn Huynen, Dries Vande Ginste

Ghent University - imec, Belgium

Differential Interconnects with Integrated Equalization and Common-Mode Filtering for Broadband Signal Integrity Enhancement in High-Speed PAM-4 Signaling

15:00

Marco Occhiali (1), Aurora Sanna (2), Simona Cucchi (2)

(1) Ansys Italia, Italy; (2) STMicroelectronics, Italy

Impact of Port Type in S-Parameter Extraction of Package and PCB High-Speed Interconnections

15:20

Andrea Gaetano Chiariello (1), Giulia Di Capua (2), Antonio Maffucci (2), Nicola Femia (3)

(1) University of Campania, Italy; (2) University of Cassino and Southern Lazio, Italy; (3) University of Salerno, Italy

Models and Methods for the Analysis of PCB Crosstalk in Switch-Mode Power Supplies

15:40 – 15:50 **IEEE TC-EDMS**

Kemal Aygün

Intel Corporation, USA

Activity of the IEEE EDMS Technical Committee

15:50 – 16:50 **POSTER SESSION**

Chairs: Antonio Maffucci and Stefano Grivet-Talocia

15:50 – 16:20 **Coffee-Break**

P-01

Jose Moreira (1), Sergey Churkin (2), Margarita Kirillova (2)

(1) Advantest, Germany; (2) Radiogigabit, Armenia

A Dual-Polarized Quad-Ridged Waveguide Antenna for OTA Near-Field ATE Socket in 5G-FR2 band

P-02

Simona Cucchi, Aurora Sanna

STMicroelectronics, Italy

Advanced package decoupling study for power integrity optimization of high-end digital devices

P-03

Soazig Le Bihan (1), Tristan Dubois (2), Jean-Baptiste Begueret (2), Marc Gatti (1), Adil El Abbazi (1), Pierre Amblard (2)

(1) THALES Avionics, France; (2) IMS Bordeaux, France

Methodology for optimizing Ethernet links at 10 and 25Gbps for critical systems in the aerospace environment

P-04

Jose Enrique Hernandez-Bonilla (1), Golzar Alavi (1), Torsten Reuschel (2), Cheng Yang (3), Christian Schuster (3)

(1) Robert Bosch GmbH, Germany; (2) University of New Brunswick, Canada; (3) Hamburg University of Technology, Germany

Uncertainty Quantification of the Insertion Loss of an Automotive PCB Stripline

P-05

Gyeongchan Jang (1), Jiseong Kim (2), Hyun Ho Park (3), Eakhwan Song (4)

(1) Vatech, South Korea; (2) Korea Advanced Institute of Science and Technology, South Korea; (3) University of Suwon, South Korea; (4) Kwangwoon University, South Korea

Segmented Cavity Design for Suppression of Cavity-to-Via Coupling in High-Speed Transmission Lines of Multi-Layer Printed Circuit Boards

P-06

João Pinho Oliveira, Fábio Coutinho, Arnaldo Oliveira

Instituto de Telecomunicações, Universidade de Aveiro, Portugal

On the Performance Analysis of Automatic Gain Control Module in Quantized OFDM 5G Systems

P-07

Rahul Kumar, Manish Bansal

STMicroelectronics Pvt Ltd, India

Complete System Analysis of High Speed Serial Interfaces of data rate up to 20Gbps with IBIS-AMI Models

P-08

Hui Zhou

Ansys AB, Sweden

Automatic PCB Material Characterization Using Design of Experiments and Mixed-Integer Sequential Quadratic Programming

P-09

Nick K. H. Huang, Huai-De Tsai, Peng-Sheng Huang, Jim Lai

Hewlett Packard Enterprise, Taiwan

Validation of Switching Voltage Regulator Noise Mitigation to Signals

P-10

Jun Wang, Yan Xu, Haiyue Yuan, Yuhao Huang, Jianmin Lu, Xiuqin Chu

Xidian University, China

Analysis of Optimum Rotation Angle for Mitigating P/N Skew Based on Geometrical Method

P-11

Yuhao Huang, Tao Wei, Yuhuan Luo, Haiyue Yuan, Jun Wang, Xiuqin Chu

Xidian University, China

Analyzing Performance of Nonlinear High-Speed Links Based on Least Square Method

17:00 onwards **City Tour**

From modern *Parque das Nações* to ancient *Belém* quarter

09:00 – 09:40 **KEYNOTE**

Solving the Challenges of High-Speed/High-Bandwidth Interconnects for Future System-in-Packages

With the emergence of new applications such as artificial intelligence, future electronic systems need to provide increasingly improved performance. One area where the performance demand has been scaling very aggressively is for interconnecting different components by means of system-in-packages with high-speed/high-bandwidth signaling. To address this demand, future system-in-package architectures and designs require innovations in package technologies, high-speed signaling analysis and validation methods and tools, and standardization.

This presentation will review some of the recent developments in electronic packaging from scaling of traditional technologies to new advanced packaging technologies for both on- and off-package interconnects. It will also summarize some of the key challenges and solutions for the corresponding electrical methodologies and metrologies that can be used for design, analysis, and validation of such packages. Finally, some recent advances on standardization of on-package high-speed signaling interconnects will be presented with some thoughts on future scaling.

Kemal Aygün

Intel Corporation, Chandler (AZ), USA

Kemal Aygün received the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Urbana, IL, USA, in 2002. In 2003, he joined the Intel Corporation, Chandler, AZ, USA, where he is currently an Intel Fellow and manages the High Speed I/O (HSIO) team in the Electrical Core Competency group. He has co-authored five book chapters, more than 90 journal and conference publications, and holds 91 U.S. patents. His research interests include novel technologies along with electrical modeling and characterization techniques for microelectronic packaging. Dr. Aygün was the General Chair of the 2020 IEEE Electrical Performance of Electronic Packaging and Systems Conference. He is an IEEE Fellow and has been acting as a Distinguished Lecturer for the IEEE Electronics Packaging Society (EPS); a co-chair of the EPS Technical Committee on Electrical Design, Modeling and Simulation; and an associate editor for the IEEE Transactions on Components, Packaging and Manufacturing Technology.

SESSION 3

09:40 – 10:20 **ELECTRO-THERMAL MODELING**

Chair: Joana Catarina Mendes

09:40

Sarah Sibilia (1), Francesco Siconolfi (1), Antonio Maffucci (1), Gaspare Giovinco (1), Isaac Appiah Otoo (2), Francesco Bertocchi (3), Sergio Chiodini (3)

(1) University of Cassino and Southern Lazio, Italy; (2) University of Eastern Finland, Finland; (3) Nanesa srl, Italy

Electro-thermal Response of Industrial-grade Graphene for Electronic Packages Applications

10:00

Lorenzo Codecasa (1), Vincenzo d'Alessandro (2), Antonio Pio Catalano (2), Ciro Scognamillo (2) Dario D'Amore (1)

(1) Politecnico di Milano, Italy; (2) University Federico II, Italy

Fast Error-Bounded MOR-based Approximation of Heat Conduction Problems in Electronics

10:20 – 10:50 **Coffee-Break**

SESSION 4

10:50 – 12:30 **AI-BASED APPROACHES FOR SI/PI ANALYSIS**

Chair: Kemal Aygün

10:50

Riccardo Trinchero (1), Tommaso Bradde (1), Mihai Telescu (2) Igor Simone Stievano (1)

(1) Politecnico di Torino, Italy; (2) Univ Brest, CNRS, France

Modeling of IC Buffers from Channel Responses via Machine Learning Kernel Regression

11:10

Jan Krummenauer (1), Alex Schuler (1), Andrew Ghaly (1), Juergen Goetze (2)

(1) Robert Bosch GmbH, Germany; (2) TU Dortmund, Germany

Evaluating Deep Reinforcement Learning for Macromodel Synthesis

11:30

Zouhair Nezhi (1), Marcus Stiemer (1), Morten Schierholz (2), Christian Schuster (2)

(1) Helmut Schmidt University, Germany; (2) Hamburg University of Technology, Germany

Dimensional Reduction by Auto-Encoders in Machine Learning Based Power Integrity Analysis

11:50

Yutaka Uematsu (1), Soshi Shimomura (1), Yasuhiro Ikeda (2)

(1) Hitachi, Ltd., Japan; (2) Hitachi Astemo, Ltd., Japan

Abnormal-state-clustering for In-vehicle Cable Communication using Equalizer Parameters and Machine Learning Approach

12:10

Ahsan Javaid (1), Ramachandra Achar (1), Jai Narayan Tripathi (2)

(1) Carleton University, Canada; (2) Indian Institute of Technology Jodhpur, India

Prediction of Power Supply Induced Jitter via Deep Belief and Knowledge-based Neural Networks

12:30 – 14:00 **Lunch**

SESSION 5

14:00 – 15:20 **OUTREACH AND CROSS-DISCIPLINARY APPLICATIONS**

Chair: Nikhita Baladari

14:00

Fábio Coutinho (1), Hugerles Silva (1), Petia Georgieva (2), Arnaldo Oliveira (1)

(1) Instituto de Telecomunicações, Universidade de Aveiro, Portugal; (2) IEETA, Instituto de Telecomunicações, Universidade de Aveiro, Portugal

On the Performance Analysis of DL-based Data Detection Algorithms in M-QAM Satellite Links

14:20

Mounir Abdkrimi, Olivier Rossetto, Olivier Bourrion, Christophe Vescovi, Christophe Hoarau

Univ. Grenoble Alpes, CNRS, France

Modeling and Analysis of Digital-to-Analog Converter Non-Idealities in Microwave Kinetic Inductance Detectors Readout

14:40

Ricardo A. Marques Lameirinhas (1), João Paulo N. Torres (2), António Baptista (3), Maria João Marques Martins (4)

(1) Instituto de Telecomunicações & Instituto Superior Técnico, Portugal; (2) Instituto de Telecomunicações & Academia Militar, Portugal; (1) Instituto de Telecomunicações, Portugal; (4) Academia Militar, Portugal

High Sensitivity Sensors based on Slit Plasmonic Gold Nanoantennas

15:00

Akira Tsuchiya

The University of Shiga Prefecture, Japan

Mean-Free-Path-Based Evaluation of Size Effect and Anomalous Skin Effect in On-Chip Interconnects under Cryogenic Environment

15:20 – 15:50 **Coffee-Break**

15:50 – 17:20 **INDUSTRY FORUM**

Moderators: Stefano Grivet-Talocia and Christian Schuster

Kemal Aygün – *Intel Corporation, USA*

Heidi Barnes – *Keysight Technologies, USA*

Olivier Bayet – *STMicroelectronics, France*

Xiaomin Duan – *IBM, Germany*

Vaishnav Srinivas – *Qualcomm, USA*

19:00 onwards **Gala Dinner**

***Casa do Alentejo* restaurant**

SESSION 6

09:30 – 10:30 **COUPLING CHARACTERIZATION AND REDUCTION**

Chair: Igor S. Stievano

09:30

Yi Zhou, Bobi Shi, Thong Nguyen, Haofeng Sun, Jose E. Schutt-Aine

University of Illinois at Urbana-Champaign, USA

Signal and Power Integrity Co-Simulation of Chiplet-to-Chiplet Channel based on Latency Insertion Method

09:50

Francesco de Paulis (1), Carlo Olivieri (1), Alessandro Pali (2)

(1) University of L'Aquila, Italy; (2) SECO s.p.a., Italy

Time Domain Assessment of Minimum FEXT by Tabbed Line Design

10:10

Alexander Gäbler (1), Uwe Maass (1), Ivan Ndip (2)

(1) Fraunhofer IZM, Germany; (2) Fraunhofer IZM, Brandenburg University of Technology, Germany

Efficient Investigation of Coupled Lines in Quasi periodical High-density Signal Routings for HPC Applications

10:30 – 11:00 **Coffee-Break**

11:00 – 11:10 **SPONSOR PITCH**

José Pedro Borrego – *ANACOM, Portugal*

SESSION 7

11:10 – 12:10 **ELECTRICAL AND ELECTROMAGNETIC PERFORMANCE ANALYSIS**

Chair: Ivan Ndip

11:10

Jun-Bae Kim, Taeho Kim, Chang Soo Yoon, Janghoo Kim, Byungjin Kwon, Youngbong Han, Jungho Jin, Seungbae Lee, Yoo-Chang Sung, Seung-Jun Bae, Daihyun Lim, Tae-Young Oh

Samsung Electronics, South Korea

Analysis of the Effects of Power Partitioning in LPDDR4x Package for Enhanced EMC Design

11:30

Doğanay Özese (1), Mustafa Gökçe Baydoğan (1), Ahmet C. Durgun (2), Kemal Aygün (3)

(1) Boğaziçi University, Türkiye; (2) Middle East Technical University, Türkiye; (3) Intel Corporation, USA

Tree-based Sequential Sampling for Efficient Designs in Package Electrical Analysis

11:50

Yanming Zhang (1), Steven Gao (1), Lijun Jiang (2)

(1) Chinese University of Hong Kong, Hong Kong; (2) Missouri University of Science and Technology, USA

Electromagnetic Near-Field Scanning with a Spatially Sparse Sampling Strategy Utilizing Kriging-DMD

12:10 – 12:30 **Closing Session**

12:30 – 14:00 **Lunch**

14:00 – 18:00 **IBIS SUMMIT**

Chair: Markus Buecker

The IBIS Open Forum held a hybrid virtual/in-person IBIS Summit meeting following the *SPI 2024 – 28th IEEE Workshop on Signal and Power Integrity* in the afternoon of Wednesday, May 15. Intended to promote exchange of ideas and methods among users and developers of IBIS models as well as the IEEE EPS and EMC Society members, the meeting was free and open to everyone interested in the topics. This was the 26th IBIS Summit associated with events in Europe.

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